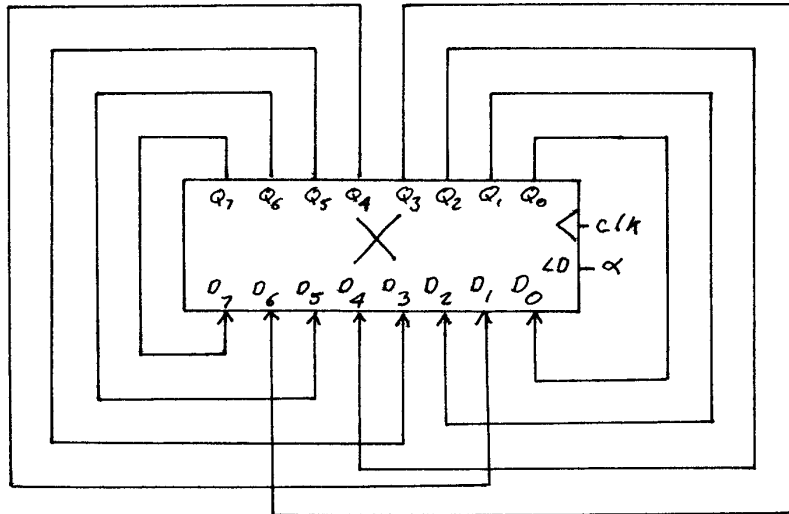


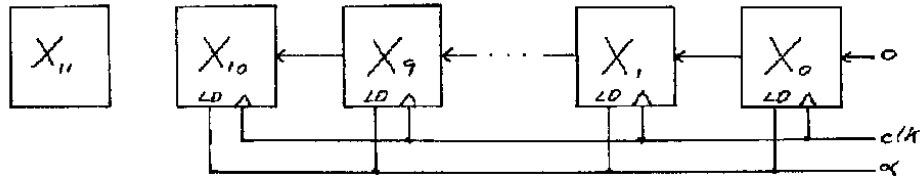
Chapter 5

5.

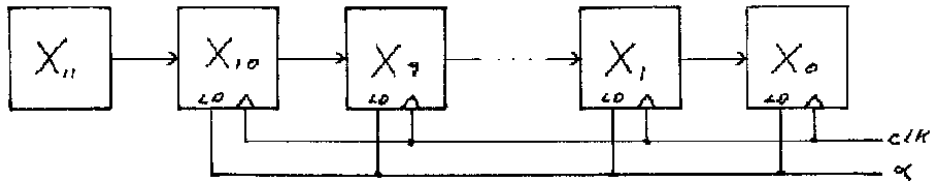


8. a) 0011 0010 0000 0100  
 b) 0100 1100 1000 0001  
 c) 0011 0010 0000 0101  
 d) 0100 1100 1000 0001  
 e) 1011 0010 0000 0100  
 f) 1100 1100 1000 0001  
 g) 1001 0000 0010 0000  
 h) 0000 1001 1001 0000

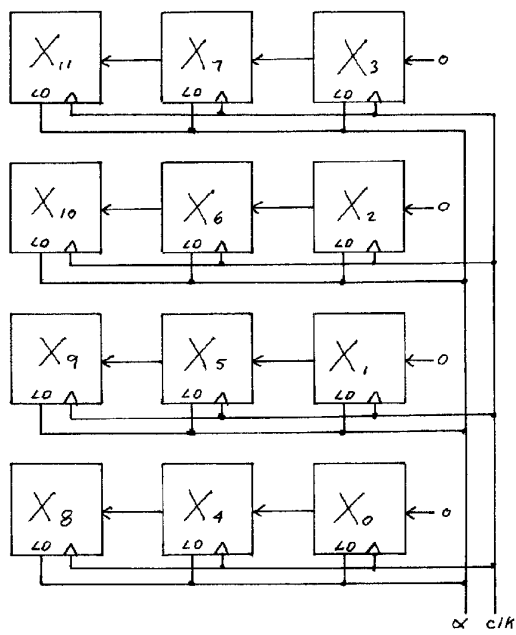
12. a)



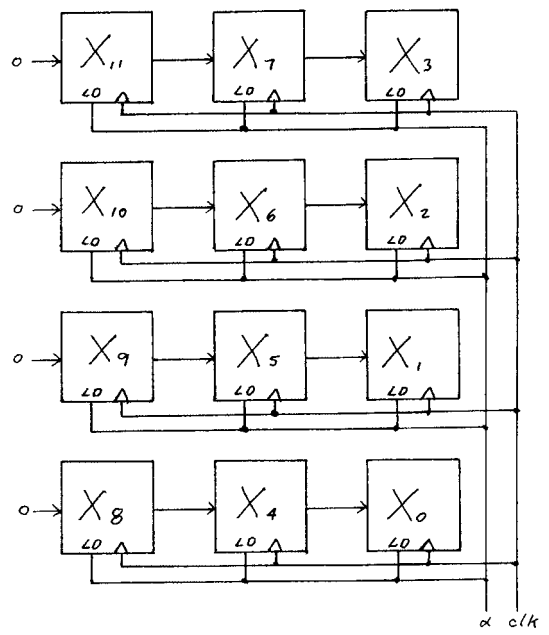
b)



c)

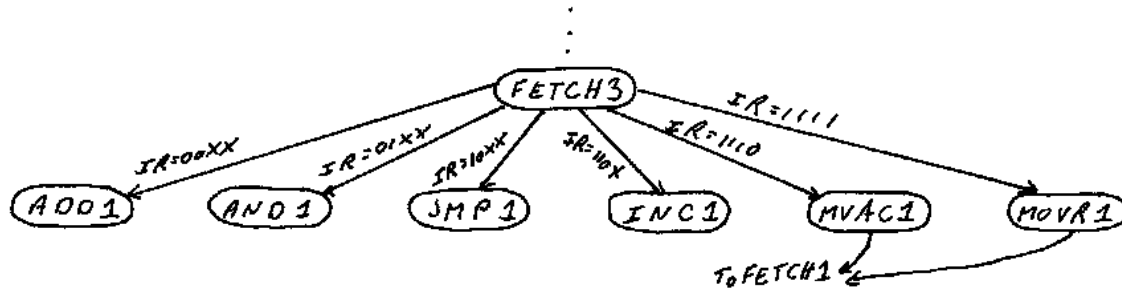


d)



## Chapter 6

10. (*IR* must have 4 bits instead of 2.)

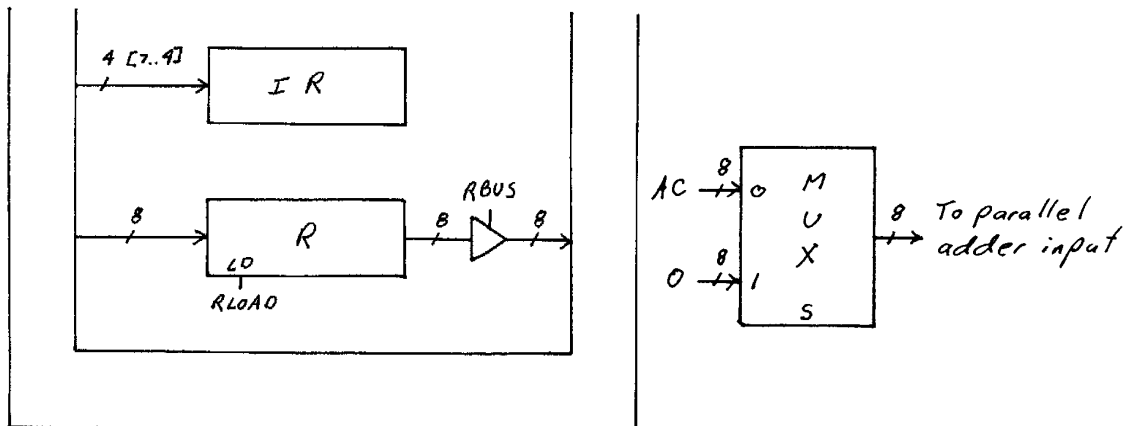


FETCH3:  $IR \leftarrow DR[7..4], AR \leftarrow DR[5..0]$

MVAC1:  $R \leftarrow AC$

MOVR1:  $AC \leftarrow R$

11. i.) *IR* must have 4 bits instead of 2. It receives bus bits 7..4 as its inputs. During *FETCH3*, bit *DR*[5..4] is sent to both *IR* and *AR*. This is shown below.  
 ii) Register *R* is added to the CPU. It receives data from the bus and sends data to the bus through tri-state buffers. It requires only a *LD* signal. This is shown below.  
 iii) The ALU is modified as shown below.



12. Arbitrarily assign *MVAC1* and *MOVR1* to decoder outputs 6 and 7, respectively.

- New input to counter:  $(IR_3 \wedge IR_2 \wedge IR_1)', IR[3..2], (IR_3 \wedge IR_2 \wedge IR_1 \wedge IR_0)$ .
- Add *MVAC1* and *MOVR1* to the inputs of the OR gate driving counter *CLR*.
- New control signals  $RLOAD = MVAC1$  and  $RBUS = MOVR1$ .
- Add *MOVR1* to the inputs of the OR gate generating *ACLOAD*.

13. Test program: 0: MVAC  
1: MOVR

<b>Instruction</b>	<b>State</b>	<b>Operations performed</b>	<b>Next state</b>
MVAC	FETCH1	$AR \leftarrow 0$	FETCH2
	FETCH2	$DR \leftarrow E0H, PC \leftarrow 1$	FETCH3
	FETCH3	$IR \leftarrow 1110, AR \leftarrow 20H$	MVAC1
	MVAC1	$R \leftarrow 1$	FETCH1
MOVR	FETCH1	$AR \leftarrow 1$	FETCH2
	FETCH2	$DR \leftarrow F0H, PC \leftarrow 2$	FETCH3
	FETCH3	$IR \leftarrow 1111, AR \leftarrow 30H$	MOVR1
	MOVR1	$AC \leftarrow 1$	FETCH1