

CoE 353H-042 Spring 2002

Homework #3 Solutions

1.

IR	MAP
00	0011
01	0101
10	0111
11	1000

$$MAP = IR_1 \wedge IR_0, IR_1 \oplus IR_0, IR_0', (IR_1 \wedge IR_0)'$$

4. Test program:
- 0: ADD 4
 - 1: AND 5
 - 2: INC
 - 3: JMP 0
 - 4: 27H
 - 5: 39H

Instruction	State	Address	Micro-operations	Operations performed	Next Address
ADD 4	FETCH1	0000	ARPC	$AR \leftarrow 0$	0001
	FETCH2	0001	DRM, PCIN	$DR \leftarrow 04H, PC \leftarrow 1$	0010
	FETCH3	0010	AIDR	$IR \leftarrow 00, AR \leftarrow 04H$	1000
	ADD1	1000	DRM	$DR \leftarrow 27H$	1001
	ADD2	1001	PLUS	$AC \leftarrow 0 + 27H = 27H$	0000
AND 5	FETCH1	0000	ARPC	$AR \leftarrow 1$	0001
	FETCH2	0001	DRM, PCIN	$DR \leftarrow 45H, PC \leftarrow 2$	0010
	FETCH3	0010	AIDR	$IR \leftarrow 01, AR \leftarrow 05H$	1010
	AND1	1010	DRM	$DR \leftarrow 39H$	1011
	AND2	1011	AND	$AC \leftarrow 27H \wedge 39H = 31H$	0000
INC	FETCH1	0000	ARPC	$AR \leftarrow 2$	0001
	FETCH2	0001	DRM, PCIN	$DR \leftarrow C0H, PC \leftarrow 3$	0010
	FETCH3	0010	AIDR	$IR \leftarrow 11, AR \leftarrow 00H$	1110
	INC1	1110	ACIN	$AC \leftarrow 21H + 1 = 22H$	0000
JMP 0	FETCH1	0000	ARPC	$AR \leftarrow 3$	0001
	FETCH2	0001	DRM, PCIN	$DR \leftarrow 80H, PC \leftarrow 4$	0010
	FETCH3	0010	AIDR	$IR \leftarrow 10, AR \leftarrow 00H$	1100
	JMP1	1100	PCDR	$PC \leftarrow 0$	0000

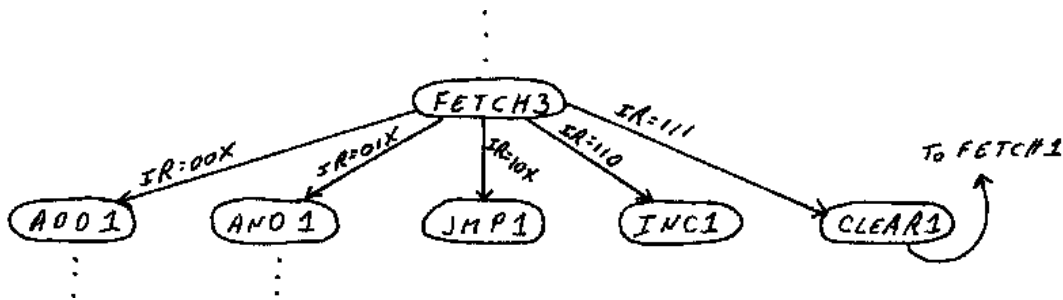
5. Use the same test program as in problem 4.

Instruction	State	Address	M1	M2	Operations performed	Next Address
ADD 4	FETCH1	0000	ARPC	NOP	$AR \leftarrow 0$	0001
	FETCH2	0001	DRM	PCIN	$DR \leftarrow 04H, PC \leftarrow 1$	0010
	FETCH3	0010	AIDR	NOP	$IR \leftarrow 00, AR \leftarrow 04H$	1000
	ADD1	1000	DRM	NOP	$DR \leftarrow 27H$	1001
	ADD2	1001	PLUS	NOP	$AC \leftarrow 0 + 27H = 27H$	0000
AND 5	FETCH1	0000	ARPC	NOP	$AR \leftarrow 1$	0001
	FETCH2	0001	DRM	PCIN	$DR \leftarrow 45H, PC \leftarrow 2$	0010
	FETCH3	0010	AIDR	NOP	$IR \leftarrow 01, AR \leftarrow 05H$	1010
	AND1	1010	DRM	NOP	$DR \leftarrow 39H$	1011
	AND2	1011	AND	NOP	$AC \leftarrow 27H \wedge 39H = 31H$	0000
INC	FETCH1	0000	ARPC	NOP	$AR \leftarrow 2$	0001
	FETCH2	0001	DRM	PCIN	$DR \leftarrow C0H, PC \leftarrow 3$	0010
	FETCH3	0010	AIDR	NOP	$IR \leftarrow 11, AR \leftarrow 00H$	1110
	INC1	1110	ACIN	NOP	$AC \leftarrow 21H + 1 = 22H$	0000
JMP 0	FETCH1	0000	ARPC	NOP	$AR \leftarrow 3$	0001
	FETCH2	0001	DRM	PCIN	$DR \leftarrow 80H, PC \leftarrow 4$	0010
	FETCH3	0010	AIDR	NOP	$IR \leftarrow 10, AR \leftarrow 00H$	1100
	JMP1	1100	PCDR	NOP	$PC \leftarrow 0$	0000

6. Use the same test program as in problem 4.

Instruction	State	Address	Control Signals	Operations performed	Next Address
ADD 4	FETCH1	0000	PCBUS, ARLOAD	$AR \leftarrow 0$	0001
	FETCH2	0001	READ, MEMBUS, DRLOAD, PCINC	$DR \leftarrow 04H, PC \leftarrow 1$	0010
	FETCH3	0010	DRBUS, ARLOAD, IRLOAD	$IR \leftarrow 00, AR \leftarrow 04H$	1000
	ADD1	1000	READ, MEMBUS, DRLOAD	$DR \leftarrow 27H$	1001
	ADD2	1001	DRBUS, ACLOAD	$AC \leftarrow 0 + 27H = 27H$	0000
AND 5	FETCH1	0000	PCBUS, ARLOAD	$AR \leftarrow 1$	0001
	FETCH2	0001	READ, MEMBUS, DRLOAD, PCINC	$DR \leftarrow 45H, PC \leftarrow 2$	0010
	FETCH3	0010	DRBUS, ARLOAD, IRLOAD	$IR \leftarrow 01, AR \leftarrow 05H$	1010
	AND1	1010	READ, MEMBUS, DRLOAD	$DR \leftarrow 39H$	1011
	AND2	1011	DRBUS, ALUSEL, ACLOAD	$AC \leftarrow 27H \wedge 39H = 31H$	0000
INC	FETCH1	0000	PCBUS, ARLOAD	$AR \leftarrow 2$	0001
	FETCH2	0001	READ, MEMBUS, DRLOAD, PCINC	$DR \leftarrow C0H, PC \leftarrow 3$	0010
	FETCH3	0010	DRBUS, ARLOAD, IRLOAD	$IR \leftarrow 11, AR \leftarrow 00H$	1110
	INC1	1110	ACINC	$AC \leftarrow 21H + 1 = 22H$	0000
JMP 0	FETCH1	0000	PCBUS, ARLOAD	$AR \leftarrow 3$	0001
	FETCH2	0001	READ, MEMBUS, DRLOAD, PCINC	$DR \leftarrow 80H, PC \leftarrow 4$	0010
	FETCH3	0010	DRBUS, ARLOAD, IRLOAD	$IR \leftarrow 10, AR \leftarrow 00H$	1100
	JMP1	1100	DRBUS, PCLOAD	$PC \leftarrow 0$	0000

7. Modified state diagram:



Modified RTL code:

FETCH3: $IR \leftarrow DR[7..5], AR \leftarrow DR[5..0]$

CLEAR1: $AC \leftarrow 0$

Microsequencer modifications:

Change the mapping hardware so that its inputs are $IR[2..0]$ and its outputs are $1, IR[2..1], (IR_2 \wedge IR_1 \wedge IR_0)$.

Register modifications:

- i) IR must have 3 bits instead of 2. It receives bus bits 7..5 as its inputs. During FETCH3, bit 5 of DR is sent to both IR and AR .
- ii) AC needs a CLR input ($ACCLR$ is a new control signal which connects to the new CLR input.)

Microcode modifications:

- i) Add micro-operation $ACCL$, which sets $AC \leftarrow 0$. Connect this bit of the microsequencer to the CLR input of AC .
- ii) Add the following to microcode memory. Set the $ACCL$ field to 0 for all other microinstructions.

State	Address	S	A	A	P	P	D	P	A	A	A	ADDR
		E	R	I	C	C	R	L	N	A	C	
		L	P	D	I	D	M	U	D	I	C	
		C	R	N	R	S				N	L	
CLEAR1	1111 (15)	0	0	0	0	0	0	0	0	0	1	0000

Verification: Test program: 0: CLEAR

Instruction	State	Address	Micro-operations	Operations performed	Next Address
CLEAR	FETCH1	0000	ARPC	$AR \leftarrow 0$	0001
	FETCH2	0001	DRM, PCIN	$DR \leftarrow 04H, PC \leftarrow 1$	0010
	FETCH3	0010	AIDR	$IR \leftarrow 111, AR \leftarrow 04H$	1111
	CLEAR1	1111	ACCL	$AC \leftarrow 00$	0000

16. PCLOAD = PCDT
TRLOAD = TRDR
PCBUS = ARPC
DRHBUS = ARDT ∨ PCDT
DRLBUS = ACDR ∨ MDR
ACBUS = DRAC ∨ RAC
READ = DRM
WRITE = MDR
MEMBUS = DRM
BUSMEM = MDR
- RBUS = ACR ∨ PLUS ∨ MINU ∨ AND ∨ OR ∨ XOR
ALUS1 = PLUS ∨ MINU ∨ ACIN
ALUS2 = MINU
ALUS3 = ACDR ∨ ACR ∨ PLUS
ALUS4 = MINU ∨ ACIN
ALUS5 = XOR ∨ NOT
ALUS6 = OR ∨ NOT
ALUS7 = AND ∨ OR ∨ XOR ∨ NOT
ACLOAD = ACDR ∨ ACR ∨ PLUS ∨ MINU ∨ ACIN ∨ ACZO ∨
AND ∨ OR ∨ XOR ∨ NOT